# Design of Low-Power High-Gain Operational Amplifier

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**Abstract:**

Operational Amplifiers are the integral part of many analog and mixed signal systems. The trend towards implementing systems with low power dissipation has created a challenging task in the design of VLSI analog circuits. Operational amplifiers are usually considered as the design bottleneck in low-voltage and low-power applications. This paper presents a two stage Operational Amplifier(Op-Amp) that achieves high-gain and low-power dissipation. The first stage is a current source load differential amplifier followed by a current mirror circuit and the output stage is a class A amplifier. This topology provides highly stable system. The proposed Op-Amp operates at 1.8V supply voltage. The Op-Amp has a mid-band gain of 72.1 dB with a bandwidth of 30.58 MHz while consuming 309.45uW of power. The proposed design has been implemented using Cadence Virtuoso Tool in 180nm CMOS technology.

***Keywords: CMOS, high-gain, low-power, Operational Amplifier, stable.***

## 1. Introduction

The complexity of the electronic systems have been increasing over the past decades. The key component in most analog electronic circuits and mixed signal system is an operational amplifier(op-amp). Operational amplifiers are the most versatile and significant building modules in the field of electronic circuits. With the scaling in the device technologies and fabrication processes, op-amps are always the challenging issue for designers.[1]

With the improved computer aided design(CAD) tools, advancements of semiconductor modelling and the advanced fabrication process, the integrated circuit market is growing rapidly and continuously. Nowadays, due to the industries trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip, CMOS technology has become dominant over bipolar technology for analog circuit design. While many digital circuits can be adapted to a smaller power supply, most existing analog circuit requires considerable change or even a redesign to accomplish the same feat. With transistor length being scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to move upon. So, when a transistor is scaled, the higher becomes its packing density, the higher its circuit speed, and the lower its power dissipation[6].

Voltage scaling plays an important role in low power circuit design. However analog circuits benefit marginally from scaling, as the minimum size transistor cannot be used in analog circuits because of noise and offset voltage constraints. Decreasing the supply voltage does not reduce the power consumption of analog circuits. This is

mainly due to the fact that the power consumption of analog circuits at a given temperature is basically set by the required signal to noise (SNR) ratio and the frequency of operation. In an effort to increase the gain of the CMOS devices, the trend in the MOSFET design industry is to shrink the gate oxide thickness, $t_{ox}$, which unfortunately reduces the tolerance at the gate for high voltage levels. So, it is advantageous to reduce the maximum voltage supply $V_{dd}$ but due to this, the ICMR and the output swing reduces.[4]

Operational Amplifiers with good DC Gains, high output swing and reasonable gain bandwidth product are usually implemented with two stage structures. The open loop gain in the CMOS technology is lower compared to bipolar counterpart due to the inherently lower transconductance of CMOS devices as well as the gain reduction due to the short channel effects that come into play for submicron CMOS processes. As a result gain enhancing methods are often required to improve the gain. This methods require more complicated circuit structures and higher power supply voltage, and may produce a limited output voltage swing. To achieve a high gain, a conventional cascode amplifier may be used, which increases the gain by stacking up transistors but this is not suitable in low voltage design as the cascode structure results in small voltage swings. Instead a multistage amplifier is widely used to boost the gain by increasing the number of gain stages horizontally. However, all multistage amplifiers suffer from the closed-loop stability problem due to the presence of multiple poles. Different frequency compensation topologies for multistage amplifiers have been used in different circuits to solve this problem.

The main aim of the paper lies on designing a two stage amplifier, with the first stage being a simple differential stage and the second stage is a common source stage, having a compensation capacitor. In between the first and the second stage a current mirror topology is used that works as a sink for the current. The current mirror sums the differential current of first stage, feeding it to the second stage by the current mirror action. This topology provides highly stable system with a high gain and it also provides low power dissipation. Thus a low power high gain operational amplifier requires designing of sub-circuits. The various transistors and components need to be configured to accomplish the required specifications. Hence, a proper design methodology is essential and the present work is an attempt in this direction.

The rest of the paper is organized as follows. Section II presents the design of low-power high-gain Operational Amplifier. Results and discussion are presented in Section III. Concluding remarks are given in Section IV.

## 2. Design of Low-Power High-Gain Operational Amplifier

The design of the Operational Amplifier is divided into three steps. The first step is to design a simple differential amplifier. Here, we are designing a current source load Differential Amplifier. The second step is designing a current mirror circuit and the third step is to design a common source class A amplifier. This topology provides highly stable system with a high gain and it also provides low power dissipation. Thus sub-circuits are designed to design the complete op-amp. The various transistors and components need to be configured to accomplish the required specifications.

2.1 Sub-Circuits

The proposed Operational Amplifier has three sub-circuits namely a differential stage, current mirror and output common source stage (also called Class A amplifier). The detailed description of these sub-circuits are presented in this section. Fig. 1 shows the simple block diagram of the proposed Op-Amp.

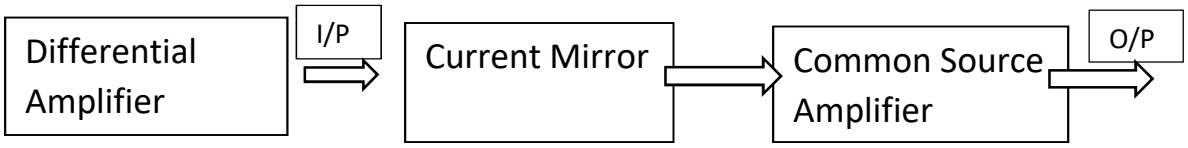


Fig. 2.1 Block Diagram of Proposed Op-Amp

2.1.1 Input Stage

A Differential Amplifier is the most versatile circuit in analog circuit design and serves as the input stage in the operational amplifier. The objective of the differential amplifier is to amplify the difference between the two input voltages. Differential Amplifier provides the most portion of the overall gain. In this Op-amp, a current source load differential amplifier is taken as the input stage. This configuration has the advantage of large input common mode range voltage. The inputs are given out of phase to the common source NMOS connected in differential form. Owing to the differential configuration, the dc gain is high but at the same time, this has the limitation of low output swing. For getting a better swing, the output stage in the form of common source stage is connected with compensation capacitor.

2.1.2 Current Mirror Circuit

The current mirror uses the principle that if the gate source potentials of two identical MOS transistors are equal, the channel currents should be equal. A current mirror replicates the input current of a current sink or current source as an output current. The output current may be identical to the input current or can be scaled version of it. Current mirror forms a cascade current sink. The maximum sinking current flows in the load capacitor which increases the output gain. It also biases the output stage transistor in the saturation region such that the output stage amplifies the single ended output of the first stage.

2.1.3 Output Stage

The output stage is implemented using a common source amplifier which is also called as class A amplifier. To reduce the output resistance and increase the current driving capability, a simple approach is to increase the bias current in the output stage. This is achieved by using a simple Class A at the output stage and using miller compensation for the second stage gain.

2.2 Design Procedure

Fig 2.2 Shows the Schematic of the proposed Op-Amp

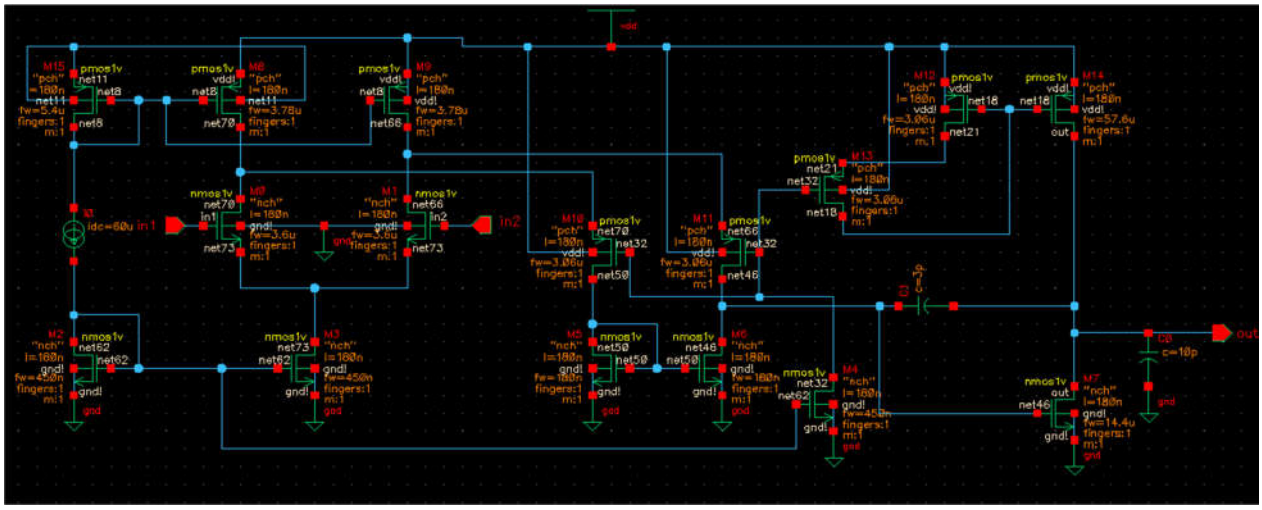

Fig 2.2 Schematic of the proposed Op-Amp

Equations (1) to (15) presents the design relationships that are used in designing the overall proposed circuit. The dc gain of the Op-Amp is given as:

$$A_v(0) = G_{MI} * R_I * R_{II} * G_{MII} \quad (1)$$

Where $A_v(0)$ is the dc gain of the op-amp, $G_{MI}$ and $G_{MII}$ are the overall transconductance of the first and the second stage of Op-Amp respectively.

First step is to compute the compensation capacitance($C_c$). It is derived from the angle equation of the Op-Amp transfer function.[4] Compensation Capacitance optimizes the phase margin of the system which makes the system more stable. The equation for compensation capacitance is given as:

$$C_C \geq 0.22C_L \quad (2)$$

Where $C_L$ is the load capacitor.

Next step is to compute the transconductance of the input transistors M1 and M2, to calculate their aspect ratios. This is given by the following equation:

$$G_{MI} = GB * C_C \quad (3)$$

Where $G_{MI}$ is the transconductance of the input stage transistor and GB is the unity gain bandwidth.

The bias current to generate biasing voltage is given by:

$$I_{Bias} = C_C * SR \quad (4)$$

Where SR is the Slew Rate.

The MOSFET current ($I_d$) in saturation region is determined by

$$I_d = k * \left(W/L\right) * (V_{GS} - V_\tau)^2 \quad (5)$$

Equation 5 is used to find the aspect ratios of M1 and M2. It is defined by equation 6.

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{ml}^2}{k_n(I_1/2)} \quad (6)$$

Using (6), the gate to source voltage of M1 is computed and is given by (7)

$$V_{GS1} = \sqrt{\frac{2I_1}{k_n^1 * (\frac{W_1}{L_1})}} \quad (7)$$

For transistor M3 to be in saturation, the source to drain saturation voltage of M3 is computed using (8)

$$V_{ICM(MAX)} = V_{DD} - V_{SD3(SAT)} + V_{TN} \quad (8)$$

Subsequently, (9) is used to determine the aspect ratios of M3 and M4 transistors

$$V_{DS3} = \sqrt{\frac{2I_3}{k_n^1 * (\frac{W_3}{L_3})}} \quad (9)$$

Equation 10 is used to calculate the saturation voltage across M5. It is given as

$$V_{ICM(MIN)} = V_{DS5(SAT)} + V_{GS1} \quad (10)$$

Then, the aspect ratio of M5 is obtained as,

$$V_{DS3} = \sqrt{\frac{2I_5}{k_n^1 * (\frac{W_5}{L_5})}} \quad (11)$$

Similarly, (12) and (13) can be used to find the aspect ratios of M6, M7 and M8,M9 respectively.

$$\frac{W_6}{L_6} = \frac{W_7}{L_7} = \frac{2 * I_{I1}}{k_P^1 * V_{SD}^2} \quad (12)$$

$$\frac{W_8}{L_8} = \frac{W_9}{L_9} = \frac{2 * I_8}{k_P^1 * V_{DSB}^2} \quad (13)$$

Since the transistors M5, M10 and M16 are configured in the current mirror circuit. The current through all this three transistors are the same and hence their aspect ratios are also same.

To compute aspect ratios of M11 and M12, the following equation is used

$$\left(\frac{W}{L}\right)_{11,12} = \frac{2I_{11}}{u_p C_{ox} V_{SD}^2} \quad (14)$$

The aspect ratio of M13 is computed using current through M13 and M12 and aspect ratio of M12.

$$\left(\frac{W}{L}\right)_{13} = \left(\frac{I_{13}}{I_{12}}\right) * \left(\frac{W}{L}\right)_{12} \quad (15)$$

Hence aspect ratios of all the transistors are computed. The summary of the aspect ratios of the transistors calculated using the above formulae is shown in Table 2.1

Table 2.1 Summary of Aspect Ratios of the transistor

| S.No. | Transistors | (W/L) |
|---|---|---|
| 1 | M1, M2 | 20 |
| 2 | M3, M4 | 21 |
| 3 | M5, M10, M16 | 2.5 |
| 4 | M6, M7, M11, M12 | 17 |
| 5 | M8, M9 | 1 |
| 6 | M13 | 320 |
| 7 | M14 | 80 |
| 8 | M15 | 30 |

## 3. Results and Discussion

Cadence Virtuoso tool is used for the performance evaluation of the proposed low power high gain op-amp at 180nm CMOS technology. The aspect ratios i.e. the W/L ratios of the transistors of the designed op-amp are calculated by the formulations as done above. The aspect ratio of the transistors M13 and M14 are large in order to achieve high gain. This also helps in getting high Unity Gain Bandwidth. This design provided an overall gain of 72.1 dB and unity gain bandwidth of 30.59 MHz. The phase margin of the system is 63.07 degrees. This makes the system highly stable. Higher phase margins imply that the closed loop poles are located far away from the origin which makes the system less oscillatory. The Input Common Mode Range (ICMR) defines the linear part of the curve where the slope is unity. The ICMR of the proposed op-amp is 0.8V to 1.6V. The slew rate is the maximum rate at which an amplifier can respond to an abrupt change of input level. The slew rate of the op-amp is 20V/us. The CMRR of the op-amp is the ratio of the common mode gain to differential mode gain. The CMRR of the proposed op-amp is found to be 136dB which is a very good value. The total power dissipated by the proposed op-amp is 309.45uW.

Fig. 3.1 shows the frequency response of the proposed Op-Amp. It is used to determine the gain and phase margin of the system. From the figure it is investigated that the gain of the Op-Amp is 72.1 dB. The high gain enables this circuit to perform efficiently in the closed loop system. It is further seen from the figure that phase margin of the system is 63 degrees. The unity gain bandwidth is 30.59 MHz.

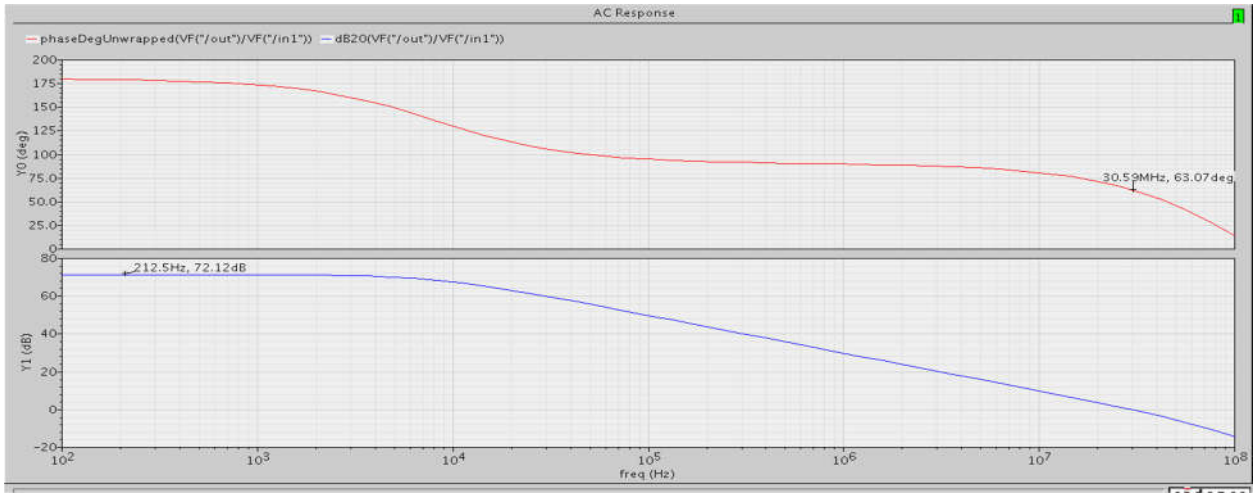


Fig 3.1 Frequency response of the proposed Op-Amp

The transient response of the proposed Op-Amp is shown in Fig. 3.2

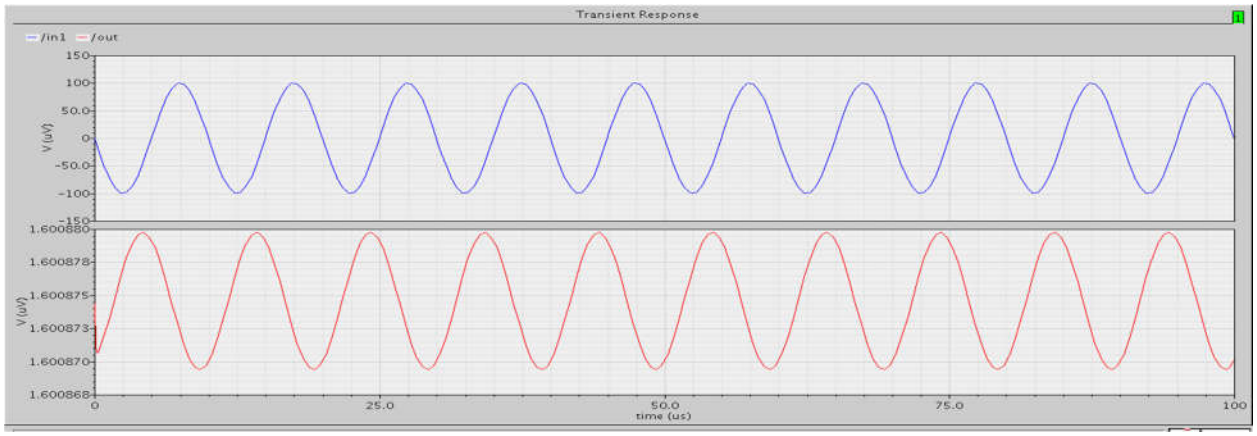


Fig 3.2 Transient Response of the Op-Amp

In order to find the Common Mode Rejection Ratio, first we find the common mode gain. For common mode gain the same AC signal is applied with 0.8V dc bias at both the terminals. The magnitude of AC source is 1 mV on both the positive and negative inputs and hence the AC signal at the output will be the common mode gain. The gain of the op-amp is 71.2 dB and the common mode gain as shown in the Fig 3.3 is -64.81 dB. Hence the CMRR of the circuit is 136.01 dB.

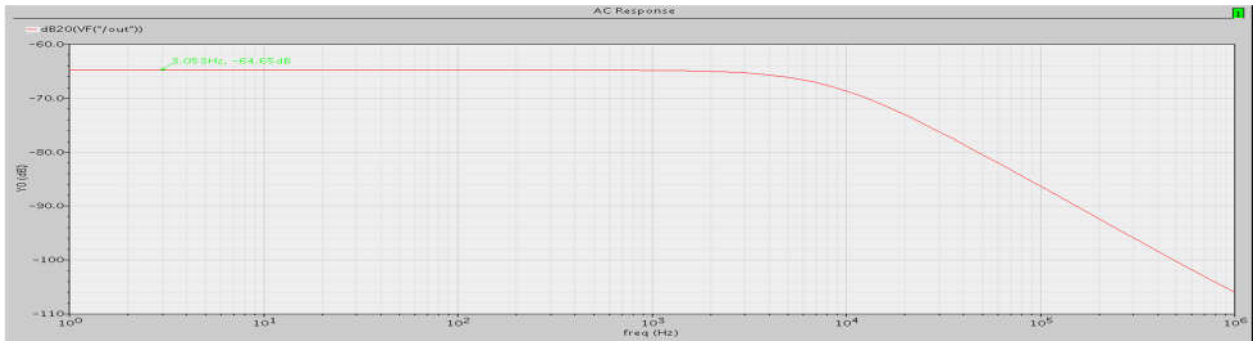


Fig 3.3 AC response of the Op-Amp showing CMRR

The performance parameters used for the Op-Amp is shown in Table 3.1

Table 3.1 Summary of performance of the designed Op-Amp

| **Parameters** | **Specifications** | **[1]** | **[4]** | **Results Obtained** |
|---|---|---|---|---|
| Technology | 180nm | 90nm | 0.5um | 180nm |
| Gain | >=60dB | 93dB | 110dB | 72.1dB |
| Phase Margin (degrees) | 60 | 70 | 95 | 63.07 |
| Gain Bandwidth | 30MHz | 11MHz | 320KHz | 30.59 MHz |
| Slew Rate | 20V/us | 20V/us | - | 20 V/us |
| ICMR | 0.8V to 1.6V | -0.9 to 1.4V | - | 0.8V to 1.6V |
| CMRR | - | - | - | 136 dB |
| Supply Voltage | 1.8V | 0.75V | 1.5V | 1.8V |
| Power Dissipation | <4mW | 1.83 mW | 27.8uW | 309.45 uW |

## 4. Conclusion

A low-power high-gain Operational Amplifier has been presented in this paper. The Op-Amp has a mid-band gain of 72.1 dB with a bandwidth of 30.59MHz while consuming 309.45uW of power. Compared to the specifications, the design achieves lower power dissipation and a better gain. Implementation of level shifter and implementation of common mode feedback circuitry can be done which reduces the input noise and enhances the system performance.

This type of Op-Amp can be used in bio-medical application because the bio-medical signal strength is low. The presented Op-Amp can also be used in low drop-out regulators where the low-power consumption is the main target.

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